1. (Thrice Amended) A method, comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a relatively wide trench and a series of relatively narrow trenches;

C1

filling said trenches with a conductive material; and

polishing said conductive material to form dummy conductors in said dummy trenches and interconnect in said series of relatively narrow trenches and said relatively wide trench, wherein said polishing comprises applying a liquid substantially free of particulate matter between an abrasive polishing surface and the conductive material.

C2

7. (Amended) The method of claim 1, wherein said abrasive polishing surface comprises particles at least partially fixed into a polymer-based matrix, and wherein said particles comprise a material selected from the group consisting of cerium oxide, cerium dioxide, aluminum oxide, silicon dioxide, titanium oxide, chromium oxide, and zirconium oxide.

9. (Twice Amended) A method, comprising:

C3

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a trench which is to receive a relatively wide interconnect feature and a series of trenches which are to receive relatively narrow interconnect features;

filling said plurality of dummy trenches with a conductive material; and

polishing said conductive material to form dummy conductors, wherein said polishing comprises applying a liquid substantially free of particulate matter between an abrasive polishing surface and the conductive material.

C4

11. (Twice Amended) The method of claim 9, wherein said polishing said conductive material is performed at a substantially uniform polish rate above said dummy trenches and said trench and said series of trenches.

15. (Amended) The method of claim 9, wherein said abrasive polishing surface comprises particles at least partially fixed into a polymer-based matrix, and wherein said particles comprise a material selected from the group consisting of cerium oxide, cerium dioxide, aluminum oxide, silicon dioxide, titanium oxide, chromium oxide, and zirconium oxide.

17. (Thrice Amended) A substantially planar semiconductor topography, comprising:

a plurality of laterally spaced dummy trenches in a dielectric layer, between a relatively wide trench and a series of relatively narrow trenches, wherein a lateral dimension of at least one of the dummy trenches is less than a lateral dimension of the wide trench and greater than a lateral dimension of at least one of the series of relatively narrow trenches;

dummy conductors in said dummy trenches and electrically separate from electrically conductive features below said dummy conductors; and

conductive lines in said series of relatively narrow trenches and said relatively wide trench, wherein upper surfaces of said conductive lines are substantially coplanar with dummy conductor upper surfaces.

Please add the following claims:

23. (Added) The substantially planar semiconductor topography of claim 17, wherein lateral dimensions of the dummy trenches are between approximately 1 micron and approximately 5 microns.

24. (Added) The substantially planar semiconductor topography of claim 17, wherein the lateral dimension of the wide trench is greater than approximately 50 microns.

25. (Added) The substantially planar semiconductor topography of claim 17, wherein the relatively narrow trenches comprise sub-micron lateral dimensions.